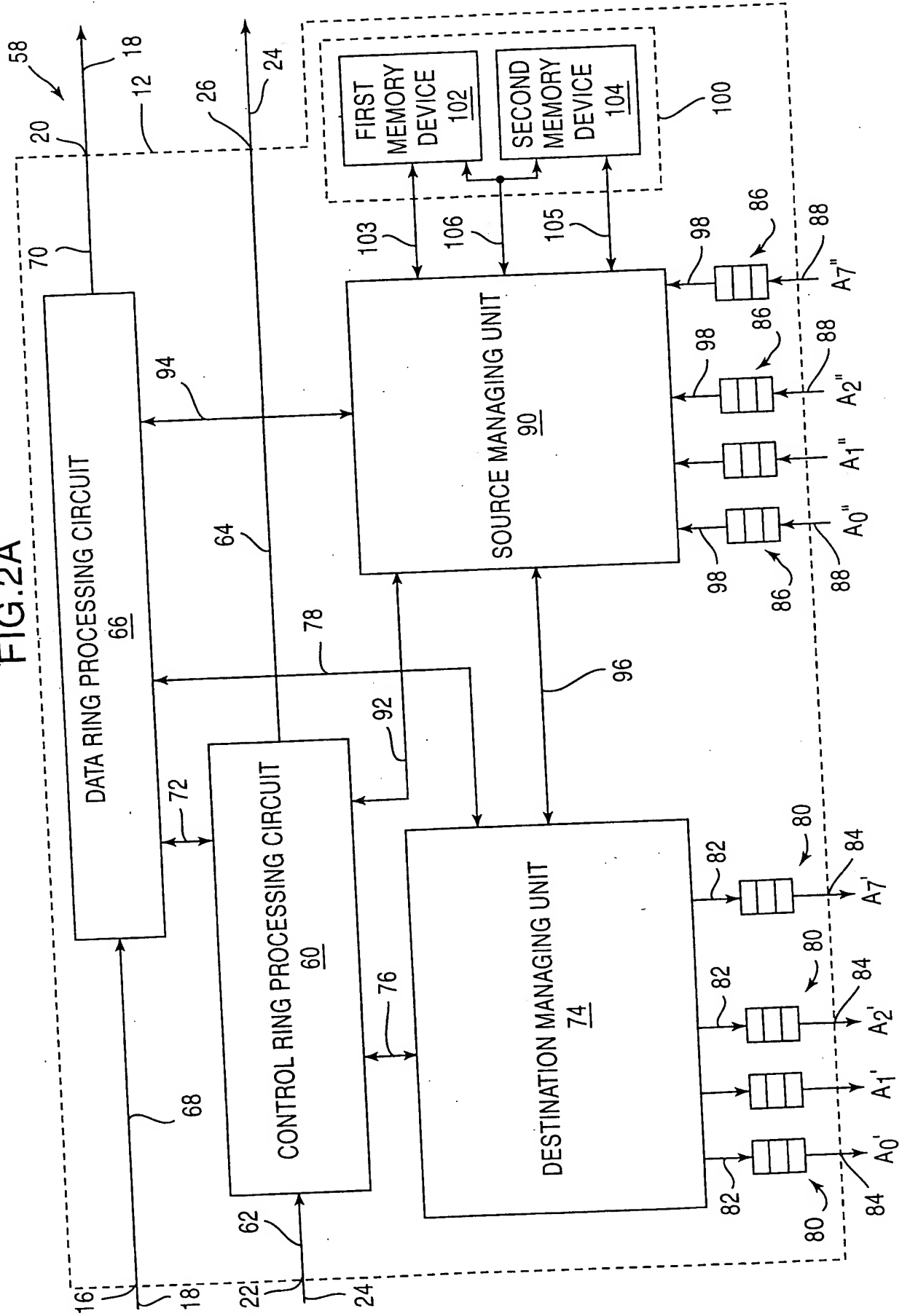


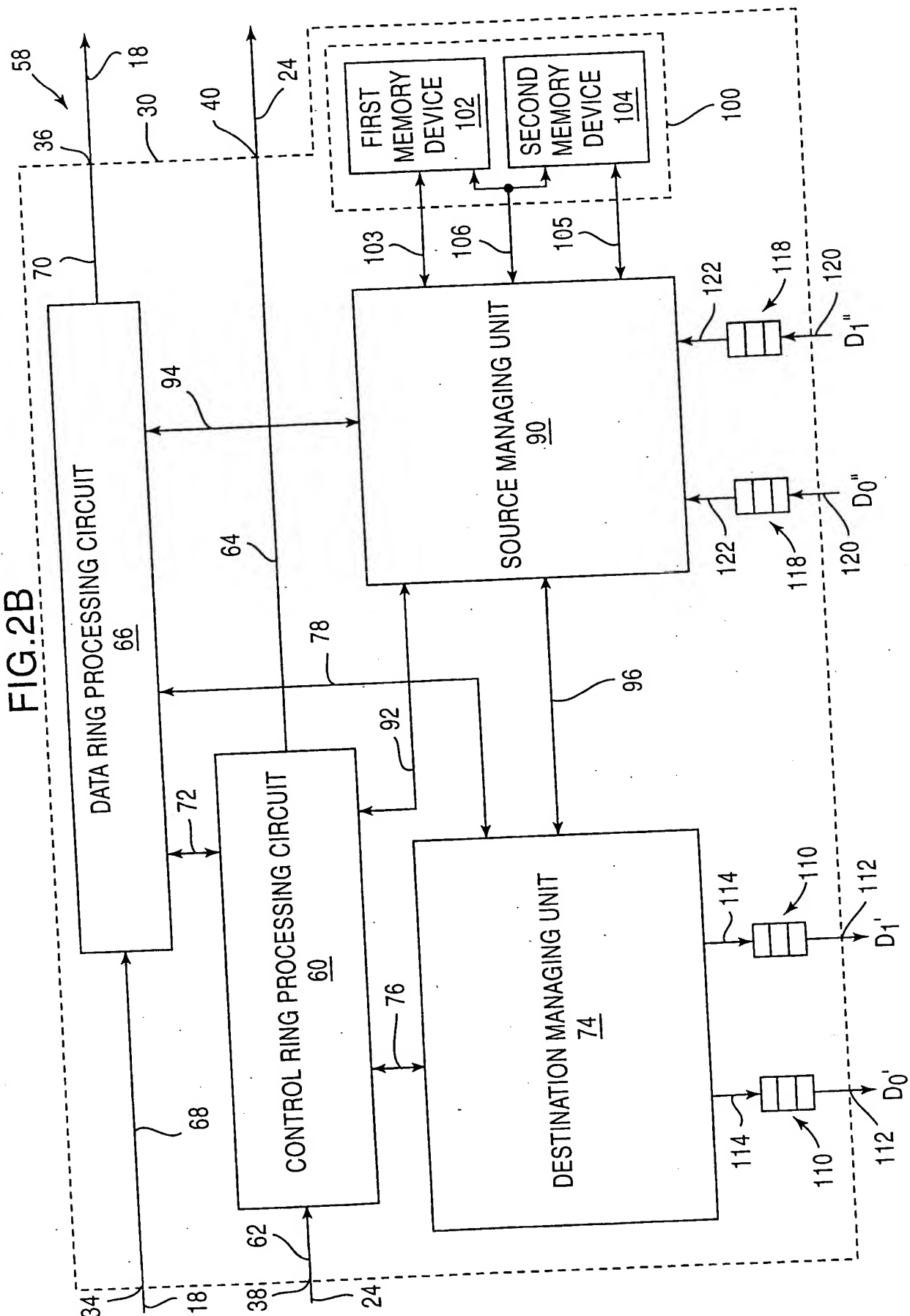
FIG. 1

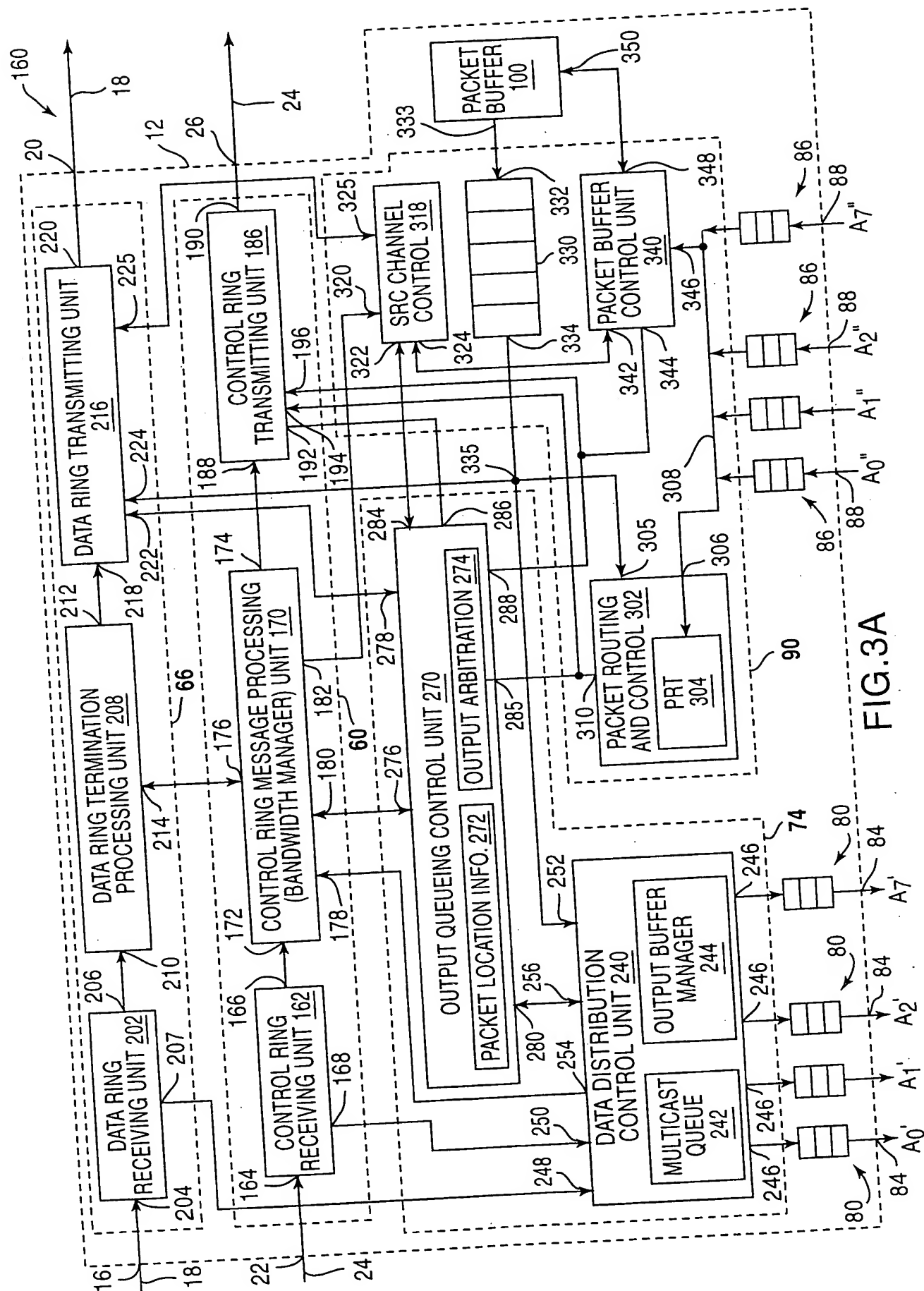
FIG. 2A

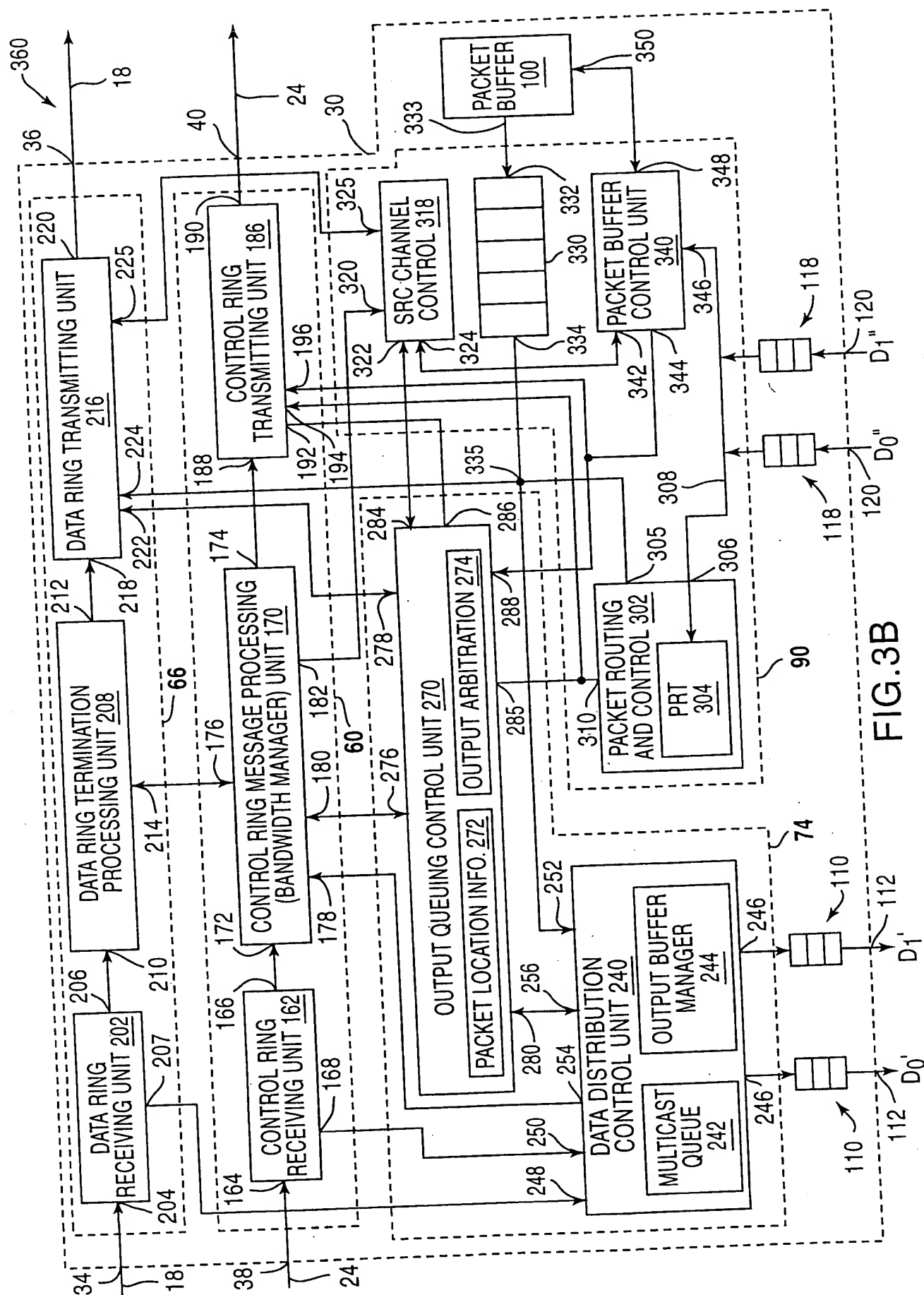


**FIG. 2B**

The diagram illustrates a data transfer system architecture. It features a **CONTROL RING PROCESSING CIRCUIT 60** and a **DATA RING PROCESSING CIRCUIT 66**. The control ring processing circuit 60 is connected to a **DESTINATION MANAGING UNIT 74** via a control line 76 and a data line 78. The data ring processing circuit 66 is connected to a **SOURCE MANAGING UNIT 90** via a data line 92 and a control line 94. Both the destination managing unit 74 and the source managing unit 90 are connected to a **DATA BUS 30**. The destination managing unit 74 includes a **DESTINATION BUFFER 110** and a **DESTINATION ADDRESS REGISTER 112**. The source managing unit 90 includes a **SOURCE BUFFER 118** and a **SOURCE ADDRESS REGISTER 120**. The system also includes a **MEMORY DEVICE 102** and a **MEMORY DEVICE 104**, which are connected to the source managing unit 90 via a **MEMORY ADDRESS REGISTER 106** and a **MEMORY DATA REGISTER 105**. The entire system is enclosed in a dashed box 100.







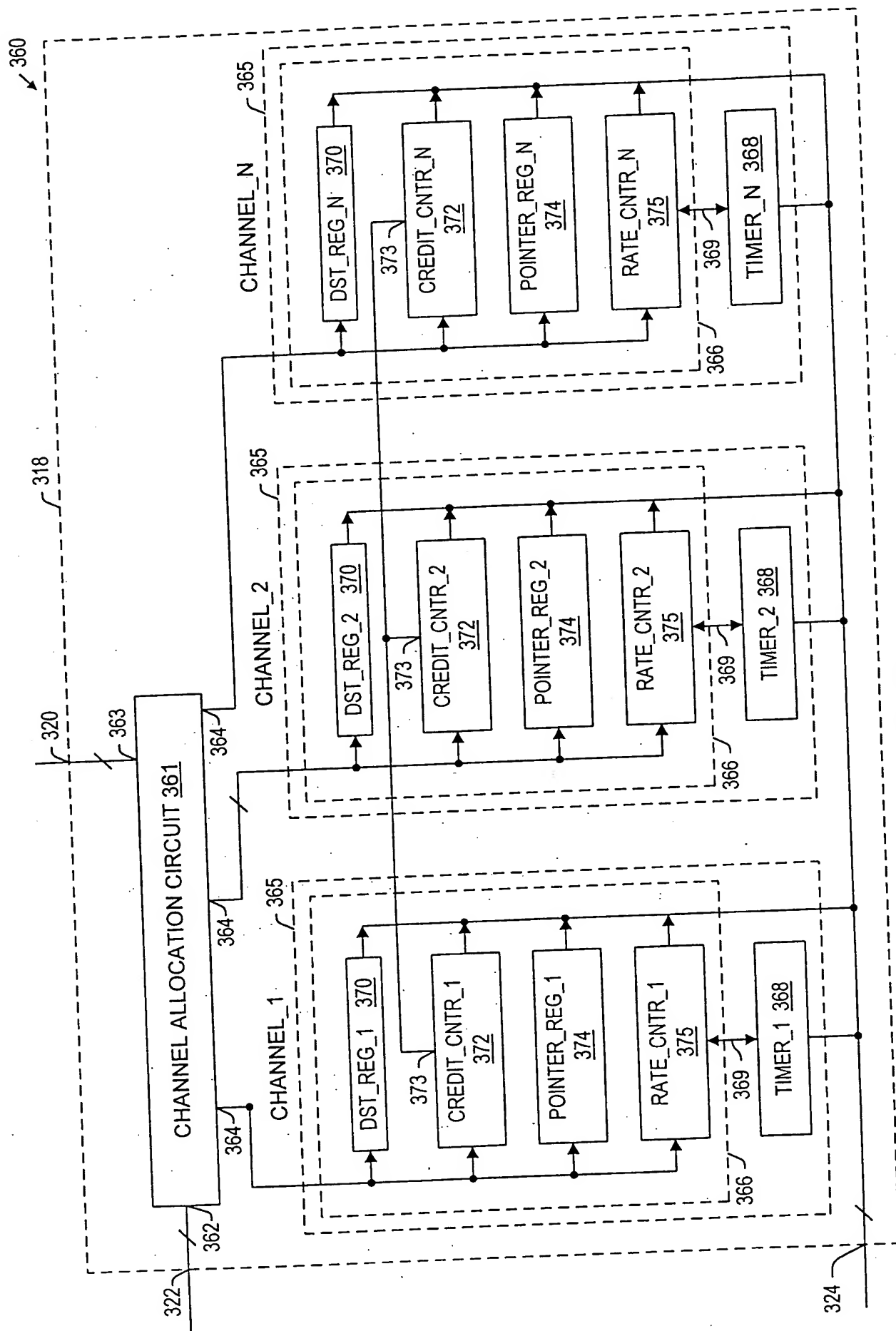


FIG. 3C

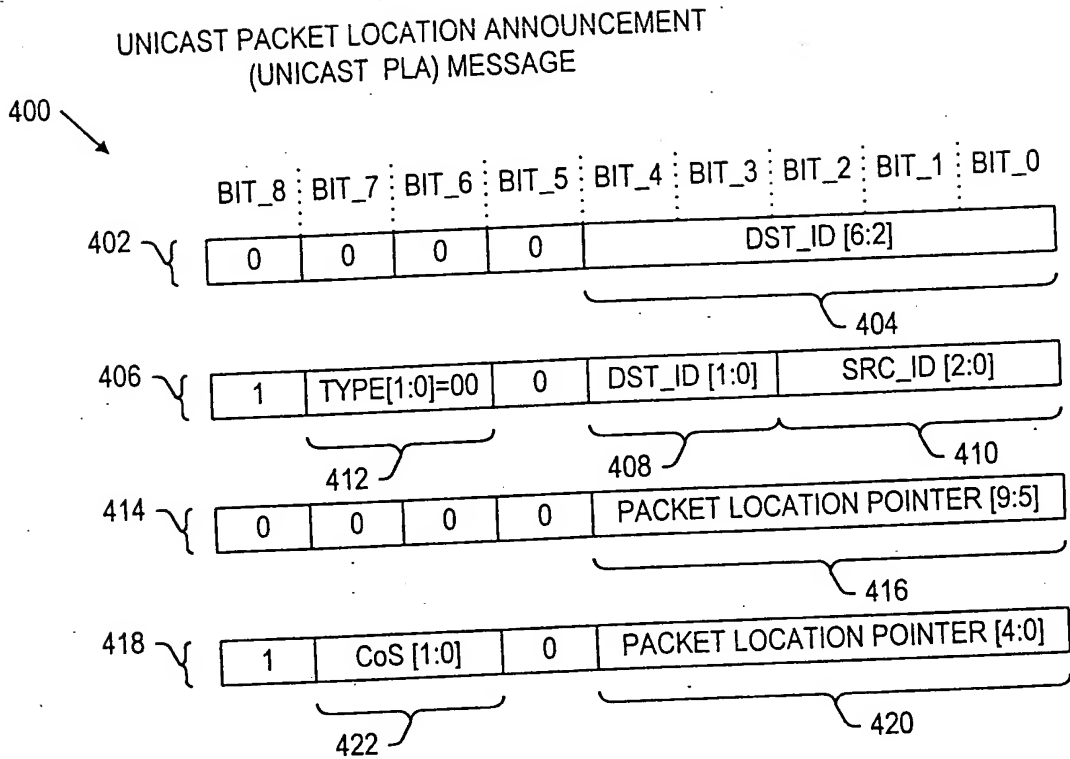


FIG. 4A

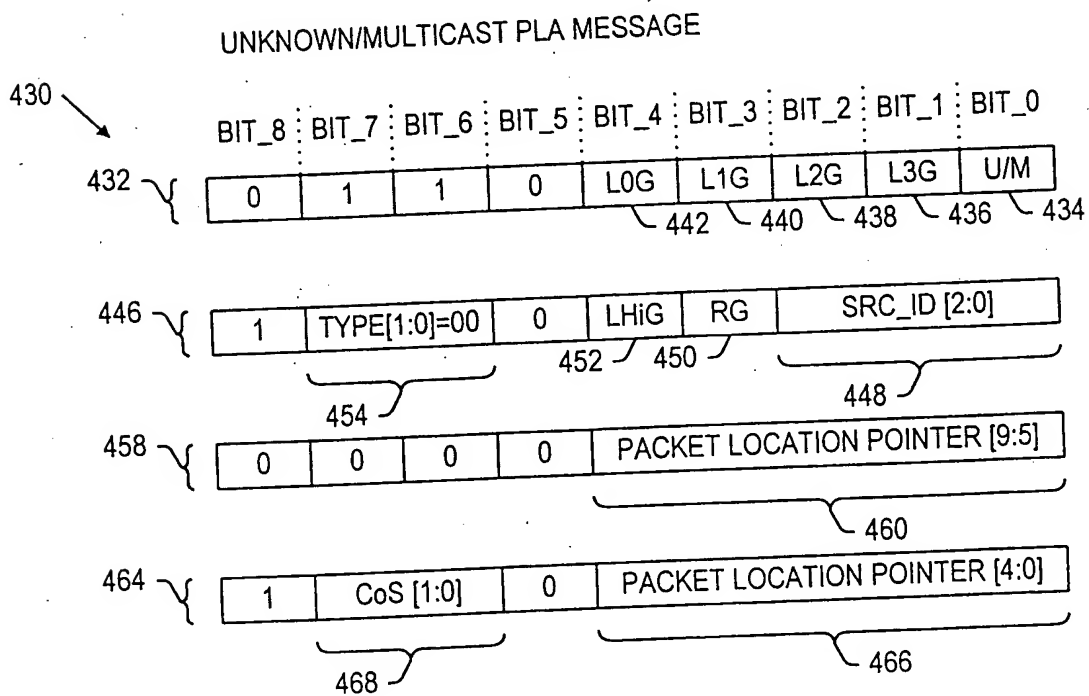


FIG. 4B

# PACKET TRANSFER NOTIFICATION (PTN) MESSAGE

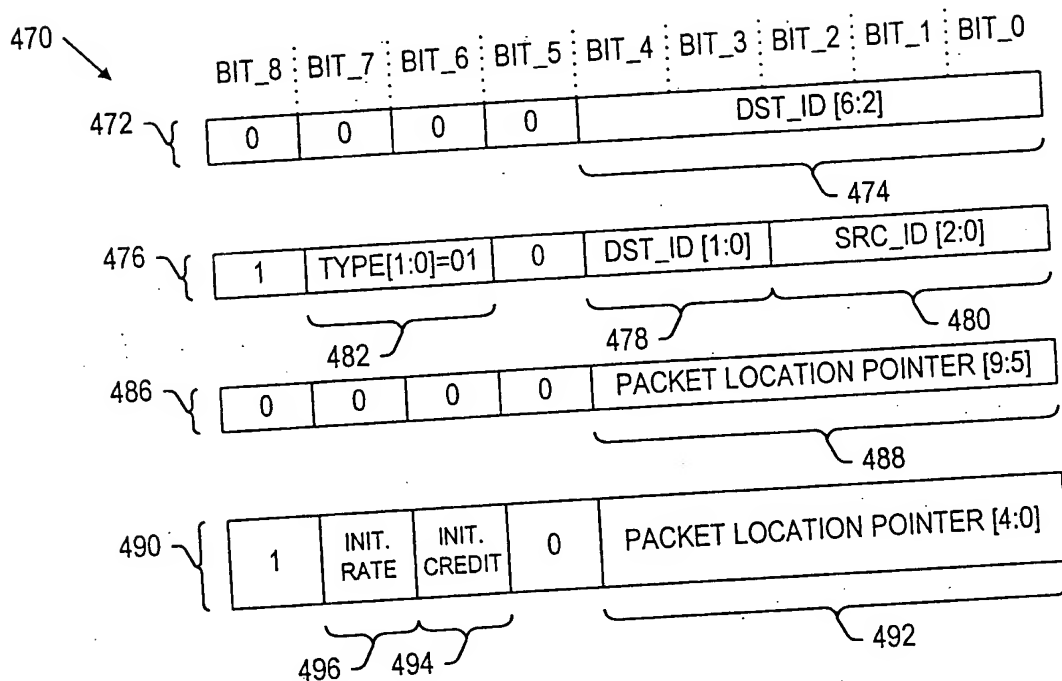


FIG. 4C

# INCREMENTAL CREDIT TRANSFER (ICT) MESSAGE

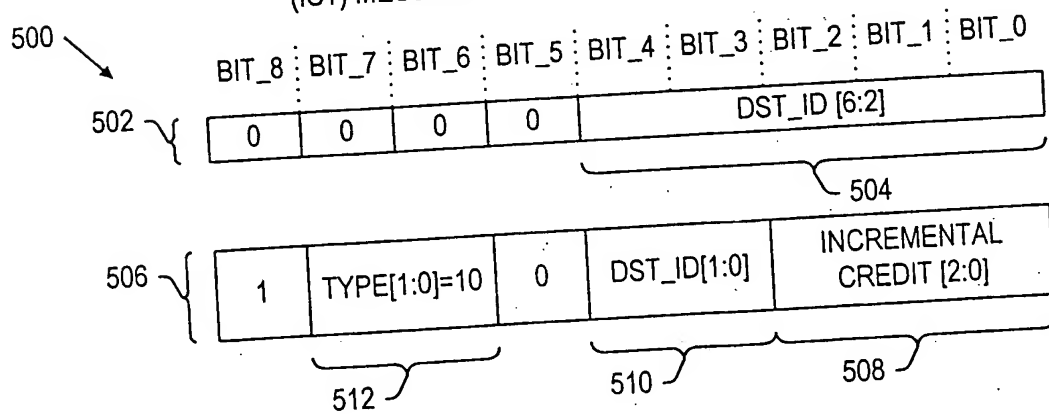


FIG. 4D



INCREMENTAL RATE TRANSFER  
(IRT) MESSAGE

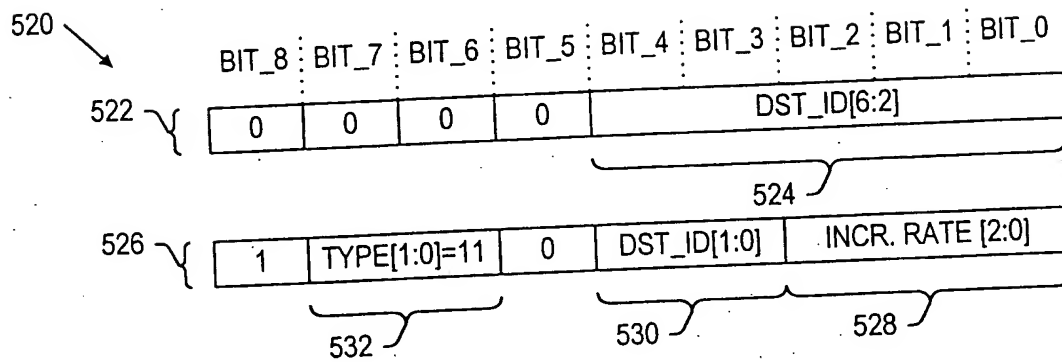


FIG. 4E

SOURCE IDENTIFICATION MAPPING TABLE

540

SRC_ID[7:0]	SOURCE
0000_0000~0000_0111	LOCAL SWITCH DEVICE 0, PORT 0 ~ PORT 7
0000_1000~0000_1111	LOCAL SWITCH DEVICE 0, RESERVED
0001_0000~0001_0111	LOCAL SWITCH DEVICE 1, PORT 0 ~ PORT 7
0001_1000~0001_1111	LOCAL SWITCH DEVICE 1, RESERVED
0010_0000~0010_0111	LOCAL SWITCH DEVICE 2, PORT 0 ~ PORT 7
0010_1000~0010_1111	LOCAL SWITCH DEVICE 2, RESERVED
0011_0000~0011_0111	LOCAL SWITCH DEVICE 3, PORT 0 ~ PORT 7
0011_1000~0011_1111	LOCAL SWITCH DEVICE 3, RESERVED
0100_0000~0100_0111	LOCAL Hi-FUNCTION DEVICE 1, SOCKET 0 ~ 7
0100_1000~0100_1111	REMOTE Hi-FUNCTION DEVICE 1, SOCKET 0 ~ 7
0101_0000~0101_1111	GATEWAY 0 ~ 15
0110_0000~0111_1111	TRUNK 0 ~ 31
1000_0000~1111_1111	MULTICAST GROUP 0 ~ 127

FIG. 5A

DESTINATION IDENTIFICATION MAPPING TABLE

570

DST_ID[7:0]	SOURCE
000_0000~000_0111	LOCAL SWITCH DEVICE 0, PORT 0 ~ PORT 7
000_1000~000_1101	RESERVED
000_1110	LOCAL SWITCH DEVICE 0, 10 Mbps PORT GROUP
000_1111	LOCAL SWITCH DEVICE 0, 100 Mbps PORT GROUP
001_0000~001_0111	LOCAL SWITCH DEVICE 1, PORT 0 ~ PORT 7
001_1000~001_1101	RESERVED
001_1110	LOCAL SWITCH DEVICE 1, 10 Mbps PORT GROUP
001_1111	LOCAL SWITCH DEVICE 1, 100 Mbps PORT GROUP
010_0000~010_0111	LOCAL SWITCH DEVICE 2, PORT 0 ~ PORT 7
010_1000~010_1101	RESERVED
010_1110	LOCAL SWITCH DEVICE 2, 10 Mbps PORT GROUP
010_1111	LOCAL SWITCH DEVICE 2, 100 Mbps PORT GROUP
011_0000~011_0111	LOCAL SWITCH DEVICE 3, PORT 0 ~ PORT 7
011_1000~011_1101	RESERVED
011_1110	LOCAL SWITCH DEVICE 3, 10 Mbps PORT GROUP
011_1111	LOCAL SWITCH DEVICE 3, 100 Mbps PORT GROUP
100_0000~100_0111	LOCAL HI-FUNCTION DEVICE 1, SOCKET 0 ~ 7
100_1000~100_1111	REMOTE HI-FUNCTION DEVICE 1, SOCKET 0 ~ 7
101_0000~101_1111	GATEWAY 0 ~ 15
110_0000~111_1111	RESERVED

FIG. 5B

# FIG.6

## CHANNEL RESOURCE PATROL MESSAGE (OR TOKEN)

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BIT LOCATION	DESCRIPTION
Header Bit	0
Bit 31 ~ Bit 28	0000
Bit 27 ~ Bit 25	SubType [2:0] = 000 (Channel Resource Patrol)
Bit 24 ~ Bit 23	Reserved
Bit 22	0
Bit 21	Reserved
Bit 20	0
Bit 19 ~ Bit 15	HiFunction Device LinkBW [4:0]
Bit 14 ~ Bit 11	HiFunction Device BBW [3:0]
Bit 10 ~ Bit 7	HiFunction Device ABW [3:0]
Bit 6 ~ Bit 2	00010
Bit 1 ~ Bit 0	Reserved

BIT LOCATION	DESCRIPTION
Header Bit	1
Bit 31 ~ Bit 29	Reserved
Bit 28 ~ Bit 24	Device 3 LinkBW [4:0]
Bit 23 ~ Bit 21	Reserved
Bit 20 ~ Bit 16	Device 2 LinkBW [4:0]
Bit 15 ~ Bit 13	Reserved
Bit 12 ~ Bit 8	Device 1 LinkBW [4:0]
Bit 7 ~ Bit 5	Reserved
Bit 4 ~ Bit 0	Device 0 LinkBW [4:0]

BIT LOCATION	DESCRIPTION
Header Bit	1
Bit 31 ~ Bit 28	Device 3 MemBBW [3:0]
Bit 27 ~ Bit 24	Device 3 MemABW [3:0]
Bit 23 ~ Bit 20	Device 2 MemBBW [3:0]
Bit 19 ~ Bit 16	Device 2 MemABW [3:0]
Bit 15 ~ Bit 12	Device 1 MemBBW [3:0]
Bit 11 ~ Bit 8	Device 1 MemABW [3:0]
Bit 7 ~ Bit 4	Device 0 MemBBW [3:0]
Bit 3 ~ Bit 0	Device 0 MemABW [3:0]

# PACKET INITIALIZATION MESSAGE

650

652

BIT LOCATION	DESCRIPTION
Header Bit	0
Bit 31 ~ Bit 28	0000
Bit 27 ~ Bit 25	SubType [2:0] = 001 (Packet Transfer Initialization)
Bit 24 ~ Bit 23	SRC DevID [2:1]
Bit 22	0
Bit 21	SRC DevID [0]
Bit 20	0
Bit 19 ~ Bit 14	Reserved
Bit 13 ~ Bit 7	Packet DST ID [6:0]
Bit 6 ~ Bit 2	00001
Bit 1 ~ Bit 0	OPERATION TYPE 00: ABORT 01: Transmit 10: RESERVED 11: RESERVED

670

BIT LOCATION	DESCRIPTION
Header Bit	1
Bit 31 ~ Bit 24	Reserved
Bit 23 ~ Bit 22	Reserved
Bit 21 ~ Bit 20	Reserved
Bit 19 ~ Bit 18	Output Control For Remote HiFunction Socket 0
Bit 17 ~ Bit 16	Output Control For Gateway 7
Bit 15 ~ Bit 14	Output Control For Port 7/Gateway 6
Bit 13 ~ Bit 12	Output Control For Port 6/Gateway 5
Bit 11 ~ Bit 10	Output Control For Port 5/Gateway 4
Bit 9 ~ Bit 8	Output Control For Port 4/Gateway 3
Bit 7 ~ Bit 6	Output Control For Port 3/Gateway 2
Bit 5 ~ Bit 4	Output Control For Port 2/Gateway 1
Bit 3 ~ Bit 2	Output Control For Port 1/Gateway 0
Bit 1 ~ Bit 0	Output Control For Port 0/Local HiFunction Socket 0 00: No Transmit; 01: Transmit Without Modification; 10: Transmit With Tag; 11: Transmit Without Tag.

FIG. 7

SOURCE DEVICE MANAGING BEHAVIOR IN RESPONSE TO RECEIVING A DATA PACKET VIA A NETWORK INPUT PORT

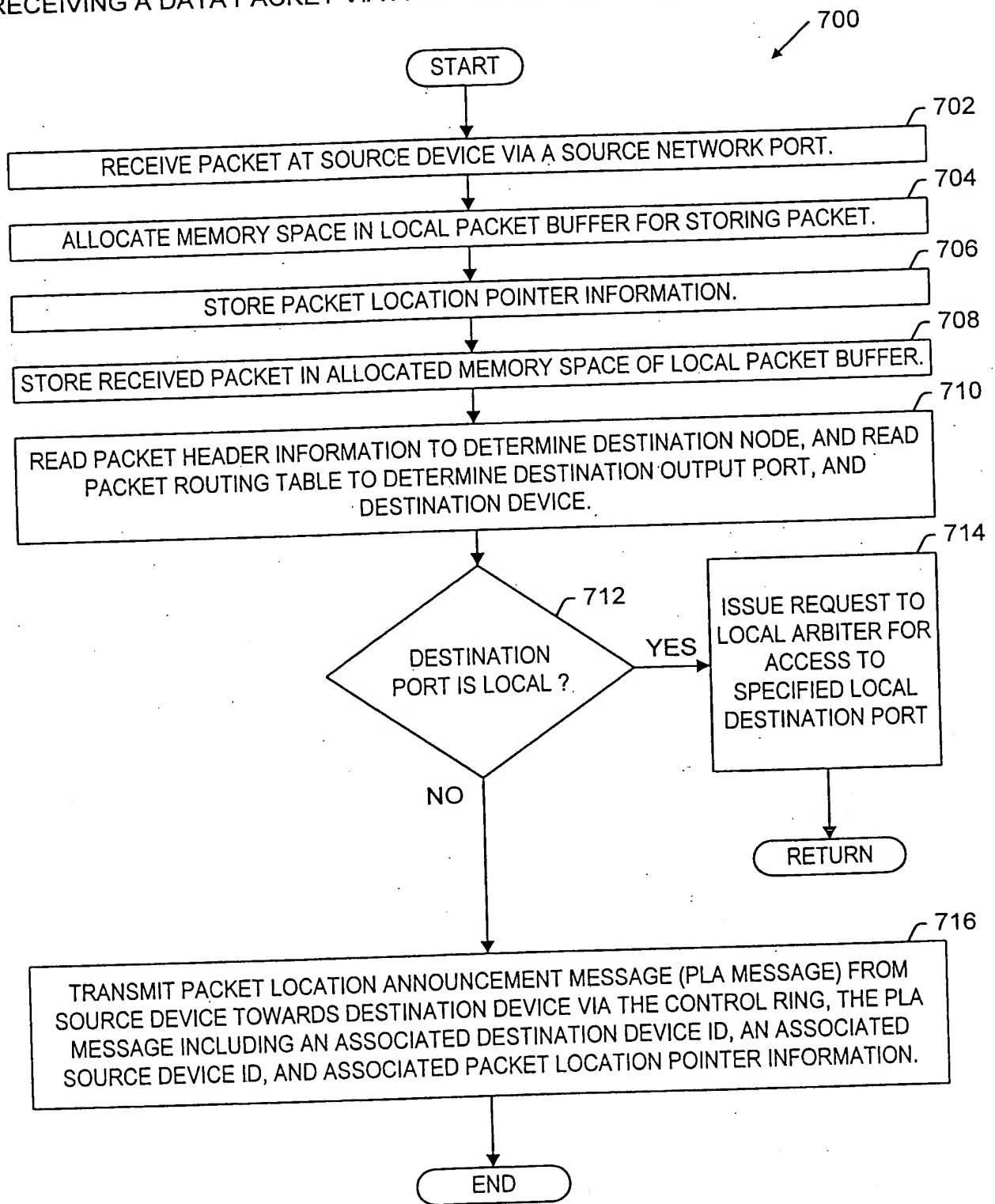


FIG. 8

DESTINATION DEVICE MANAGING BEHAVIOR IN  
RESPONSE TO RECEIVING A KNOWN UNICAST  
PACKET LOCATION ANNOUNCEMENT (PLA) MESSAGE  
FROM A SOURCE DEVICE

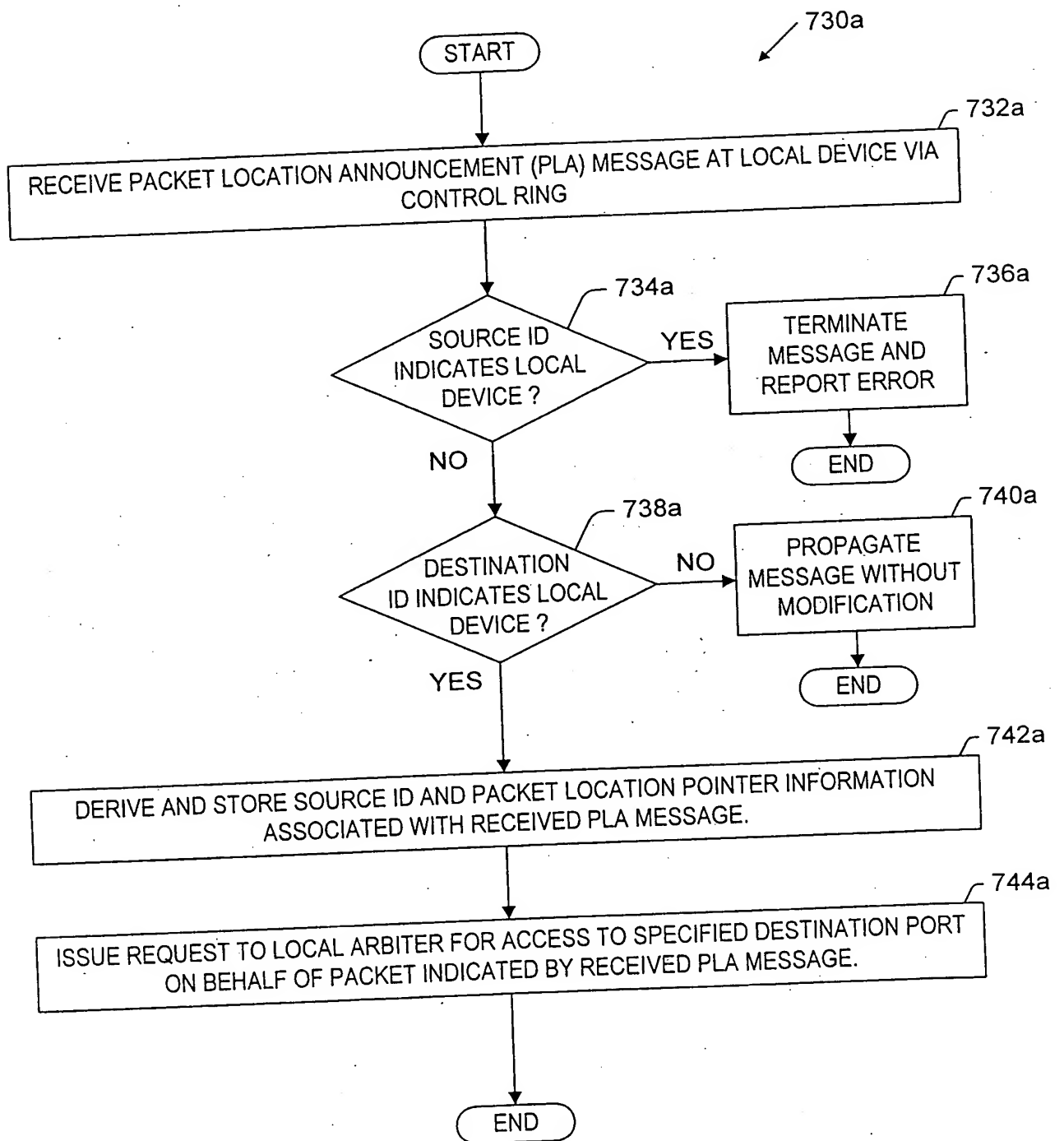


FIG. 9A





DESTINATION DEVICE  
ARBITRATION BEHAVIOR

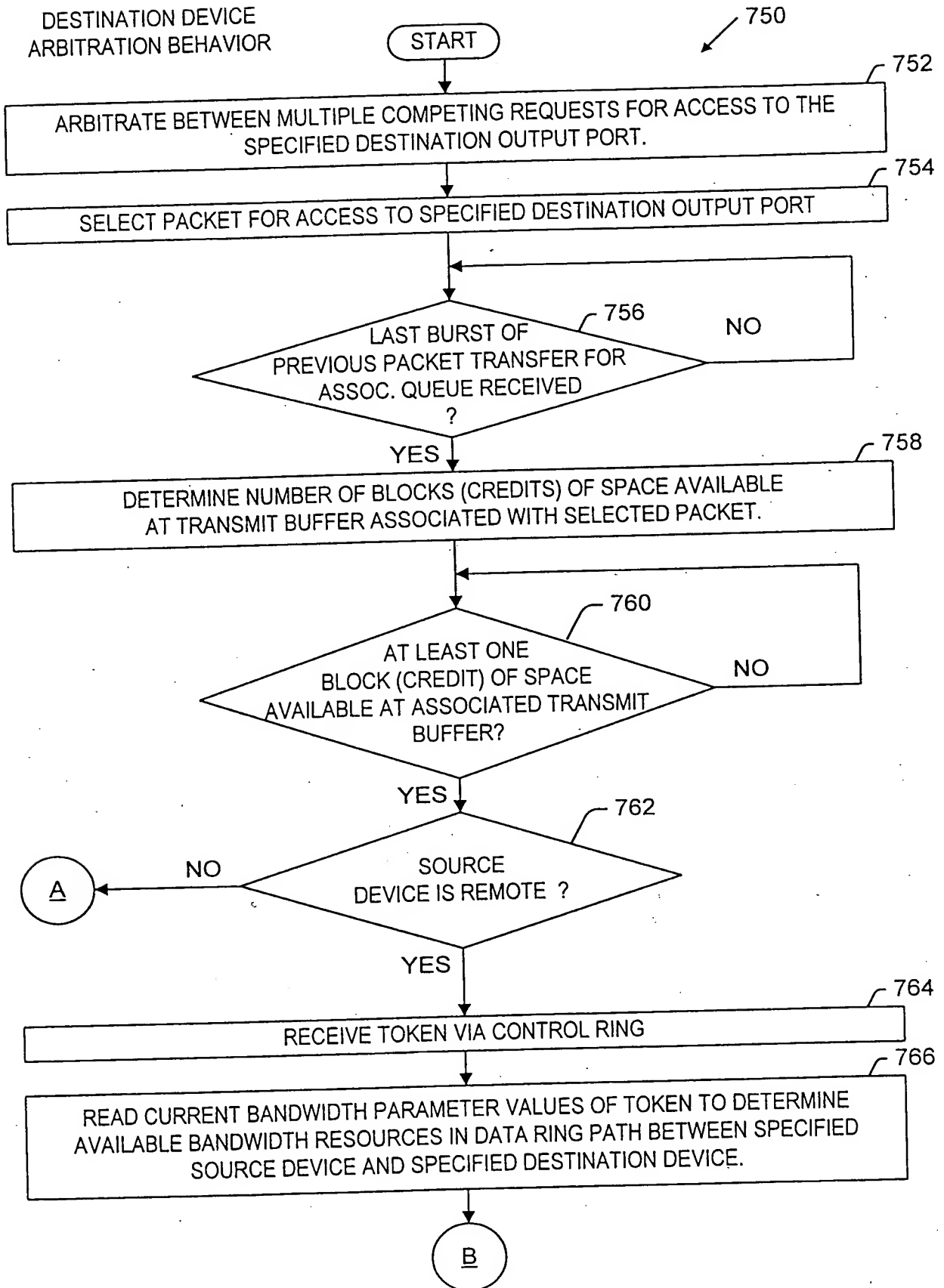


FIG. 10A

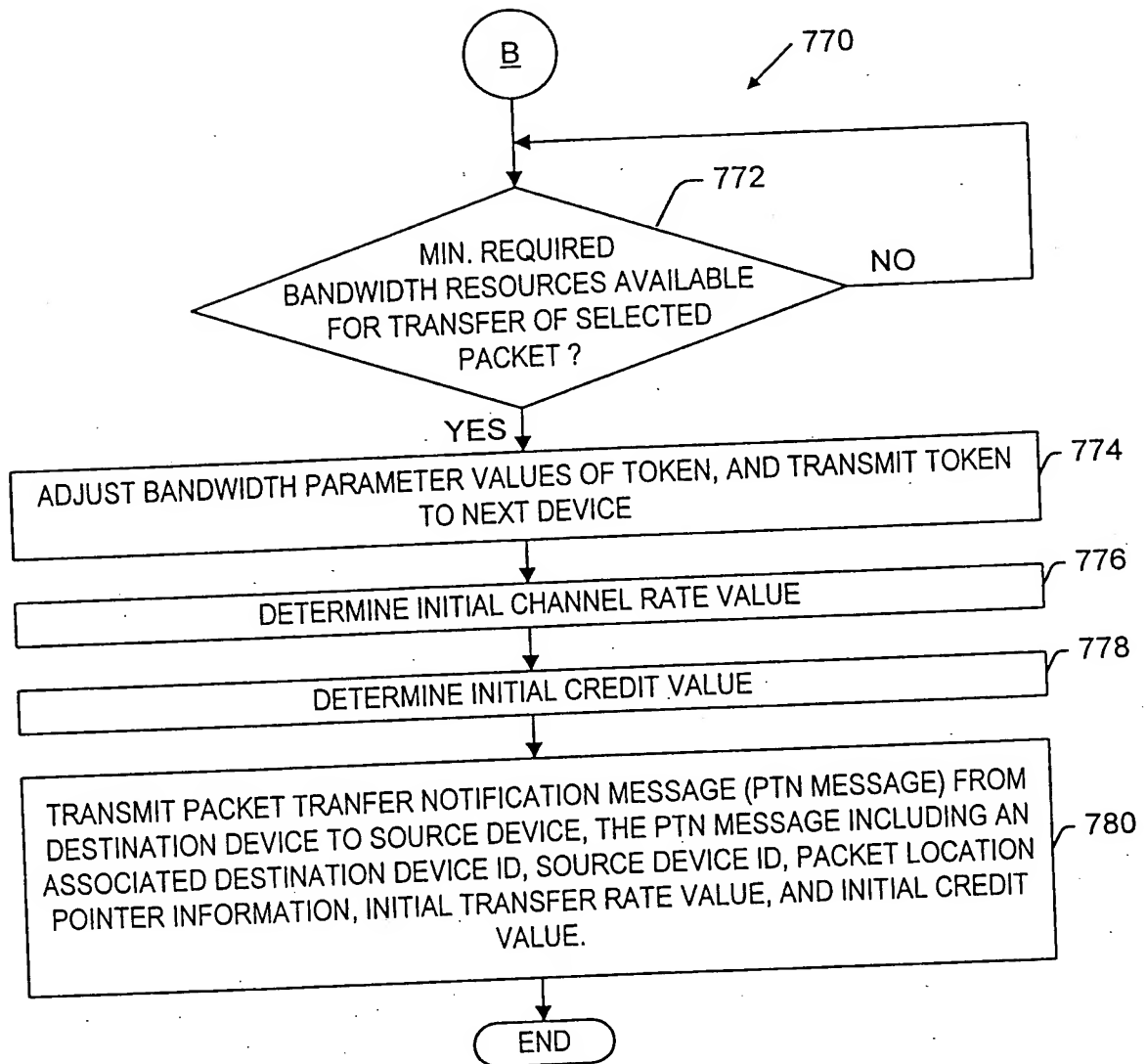


FIG. 10B

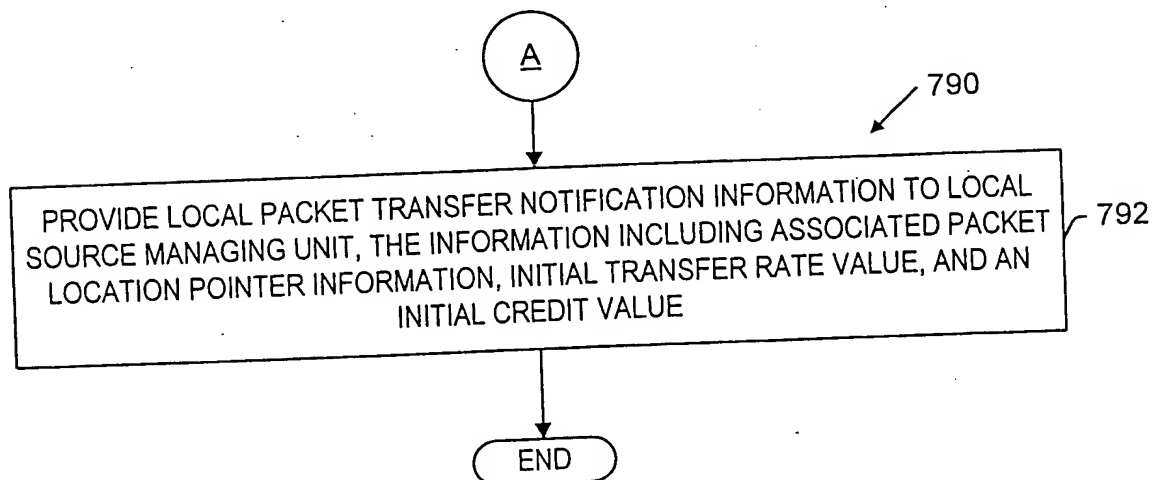


FIG. 10C

# DEVICE SOURCE BEHAVIOR IN RESPONSE TO RECEIVING A PTN MESSAGE

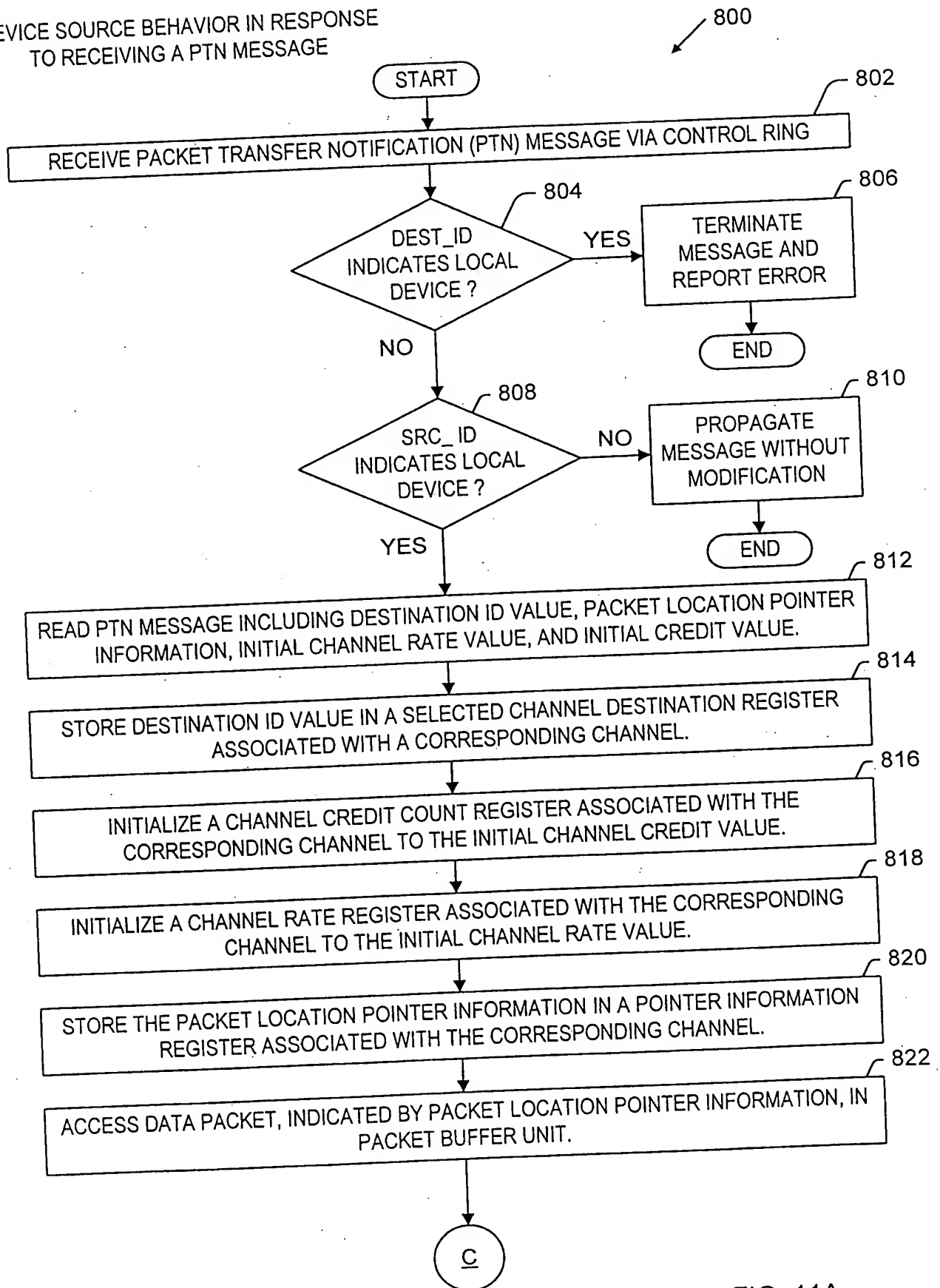


FIG. 11A

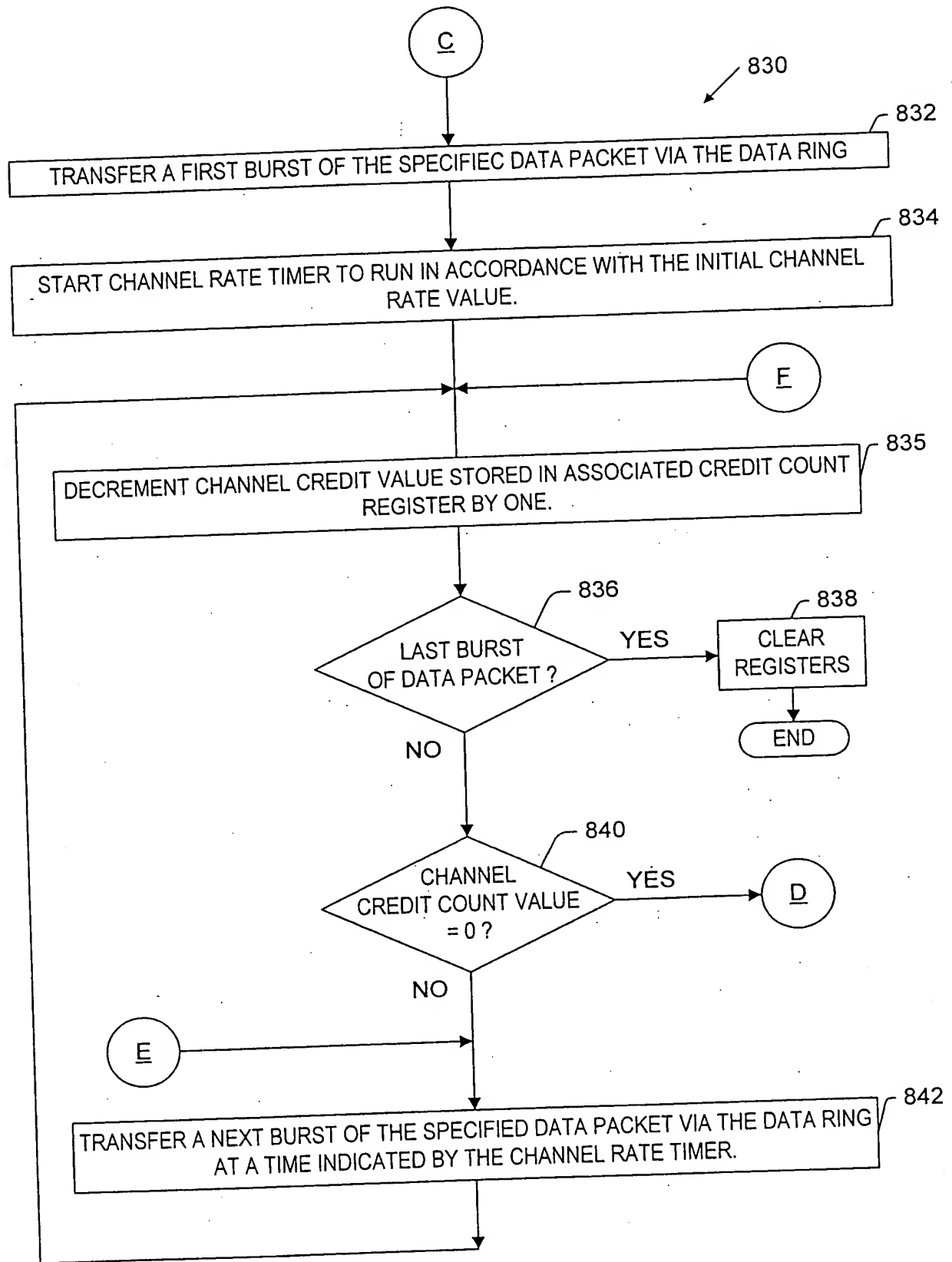


FIG. 11B

DEVICE SOURCE BEHAVIOR IN RESPONSE TO RECEIVING AN  
INCREMENTAL CREDIT TRANSFER MESSAGE (ICT MESSAGE)

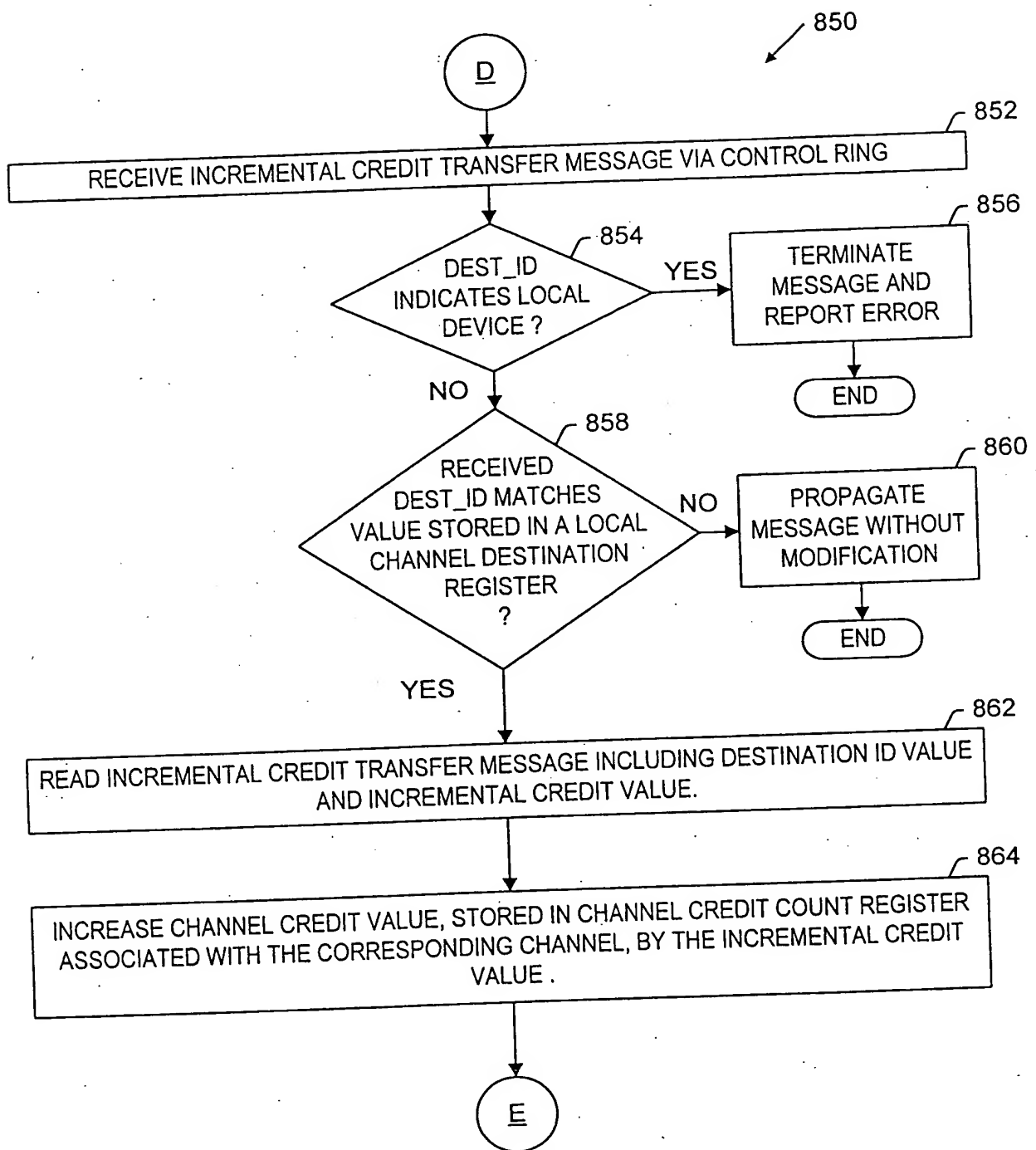


FIG. 12

DEVICE SOURCE BEHAVIOR IN RESPONSE TO RECEIVING AN  
INCREMENTAL RATE TRANSFER MESSAGE (IRT MESSAGE)

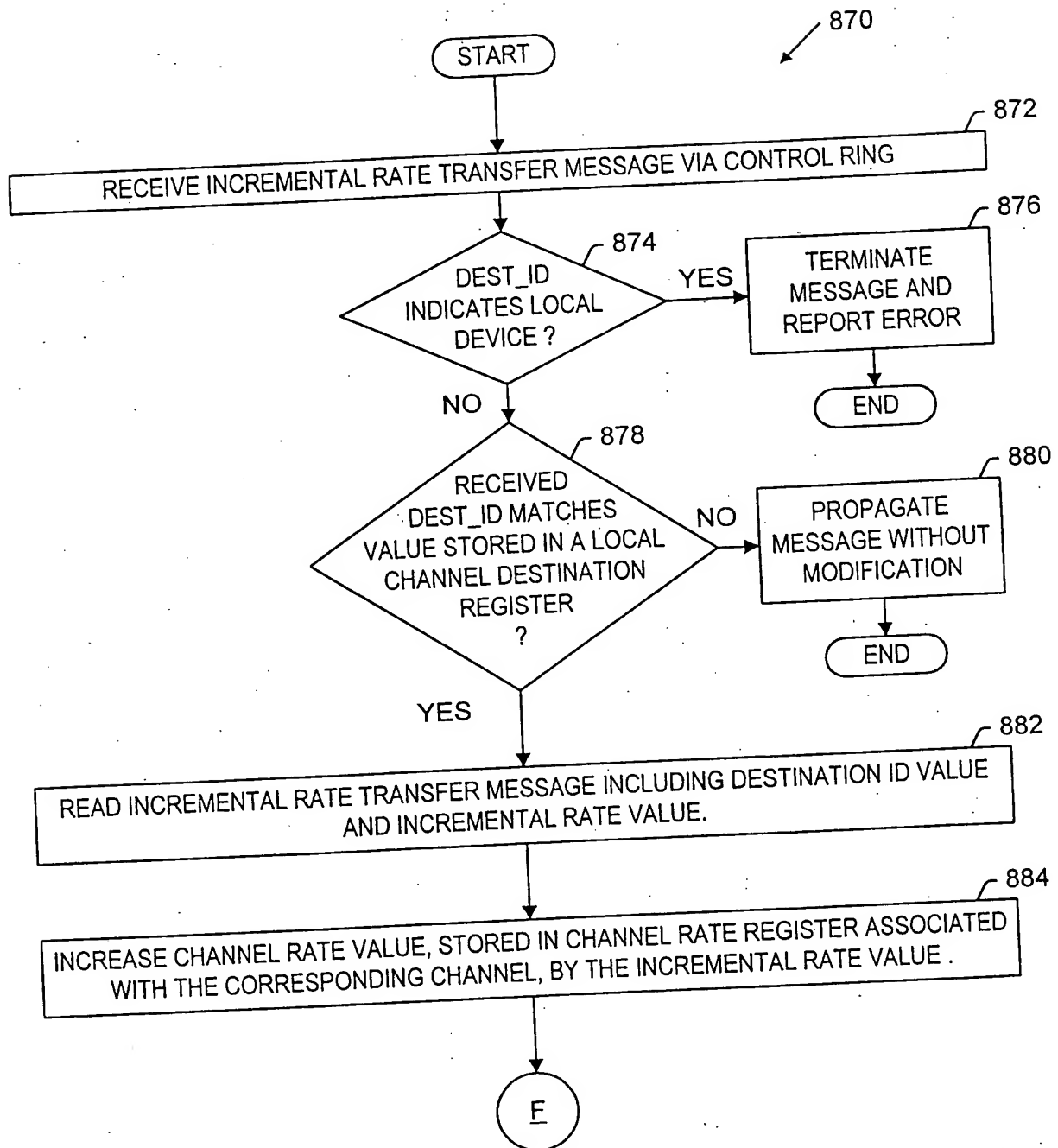


FIG. 13